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NXP and Identiv
Make IoT Applications More Accessible with Ultra-Low-Cost NFC Inlay

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In this Edition:

Daniel Dierickx
CEO & co-Founder
at e2mos
Acting Chief Editor

Over 3 decades
Chips & Embedded
Systems Market Expertise

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Ampere and Packet
Partner to Expand Adoption of eMAG™ Processors for Next-Generation Cloud and Edge Workloads

Accelerates Deployment of New Applications on High-Performance and Affordable Servers

Santa Clara, CA March 28, 2019 – Ampere™, a developer of **high-performance Arm®-based microprocessors for cloud and edge servers**, and Packet, the **leading bare metal automation platform** for developers, today announced a partnership that delivers on-demand and cost-effective bare metal access to Ampere's high-performance eMAG™ platform.

Ampere eMAG processors deliver excellent total cost of ownership (TCO) value, high-performance compute, high-memory capacity, and rich I/O to address general-purpose workloads such as web servers, containers, distributed databases and big data analytics.

"Adoption of our eMAG server platforms is growing across a diverse set of customers and applications," said Matt Taylor, senior vice president of worldwide sales and business development at Ampere. "This partnership broadens access to our platform to users looking for high-performance and cost-effective Arm-based processors to run their applications."

Packet's new c2.large.arm configuration pairs the Ampere™ eMAG processor, which features 32 Arm cores operating at 3.3 GHz, with 128GB of RAM, 480GB of SSD storage and dual 10Gbps network ports. It is available on demand for $1.00/hr from Packet's core datacenters in the US, Europe and Asia.

"Today's launch opens an exciting new chapter in our journey with the Arm ecosystem," said Jacob Smith, Packet's CMO and co-founder. "By making Ampere's powerful technology available in our bare metal public cloud, we're providing developers and enterprises alike with a sharp new tool in their infrastructure toolbox."

To showcase the role of the Arm® architecture in the fast-evolving edge computing market, the companies also announced availability of the Ampere-based systems through Packet's Edge Access Program.

About Ampere

Ampere is designing the future of hyperscale cloud and edge computing server processor architecture. Born in and built for the cloud with a modern architecture, Ampere gives customers the freedom to accelerate the delivery of the most memory-intensive applications such as artificial intelligence, big data, machine learning and databases in the cloud. The Ampere eMAG family of products delivers the highest memory throughput and lowest TCO tailored for the emerging growth of cloud computing and next-generation data centers.
For more information, visit www.amperecomputing.com

Product Brief Click Here

About Packet

Packet is the leading bare metal automation platform for developers. Its proprietary technology automates physical servers and networks without the use of virtualization or multi-tenancy, powering over 60k deploys each month across its 20+ global and three edge data centers, as well as dozens of private and on-premise locations.
To learn more, please visit www.packet.com

Supporting Quotes

Hatch
"Packet's ability to provide bare metal Arm servers based on Ampere's eMAG processor is a win for our platform, especially as we scale to meet demand," said Mikko Peltola, Director Cloud Operations at Hatch. "The combined solution helps us power our revolutionary game streaming experience in a cost-effective manner."

Arm
"We are seeing growing customer demand for Arm-based platforms as we build the infrastructure that will support a trillion connected devices," said Mohamed Awad, vice president of marketing, Infrastructure Line of Business, Arm. "The partnership between Ampere and Packet offers a new solution that provides developers and end-users with another great option for high-performance, bare-metal Arm-based servers."

Red Hat
"Red Hat has worked extensively with the Arm community to drive the adoption of common open standards and technology roadmaps, helping to bring Arm-based servers in-line with the existing datacenter experience," said Jon Masters, computer architect, Red Hat. "In collaboration with both Packet and Ampere, we're pleased to see these open standards delivered via Ampere's bare-metal Arm servers running on Packet's cloud, providing additional choice to enterprise IT organizations in not only selecting the best architecture for a given workload but also where this architecture can run."

Infineon strengthens collaboration with DENSO – DENSO becoming a shareholder

Source: https://www.infineon.com/cms/en/about-infineon/press/press-releases/2018/INFXX201811-015.html

Munich, Germany – **26 November 2018** – Infineon Technologies AG (FSE: IFX / OTCQX: IFNNY) is strengthening its long-term partnership with DENSO Corporation, a global supplier of advanced automotive technology, systems and components, to bolster its automotive business. Infineon is a global leader in semiconductor solutions for the automotive industry. Both companies aim to jointly enhance their system know-how in established and new technologies – like automated driving and electro-mobility.

Underpinning this collaboration, the Japanese company has bought an equity stake in Infineon in the range of a mid-double-digit million Euro amount.

"We would like to establish optimal semiconductor solutions for in-vehicle electronics systems through strong partnerships with semiconductor companies in order to enhance the competitiveness of automated driving and electrification systems," said **Hiroyuki Ina, Senior Executive Director of DENSO Corporation.**

"We are very pleased to expand our already well-established relationship with DENSO," said **Dr. Reinhard Ploss, CEO of Infineon.** "Our collaboration with Japan's largest and world-leading automotive system supplier is strengthening our links with the Japanese industry as well as our position in the Japanese and global semiconductor market. We welcome DENSO becoming a shareholder."

About DENSO Corporation
DENSO Corporation, headquartered in Kariya, Aichi prefecture, Japan, has approximately 220 subsidiaries in 35 countries and regions (including Japan) and **employs approximately 170,000 people worldwide.**

Consolidated global **sales for the fiscal year ending March 31, 2018, totaled US$48.1 billion.** Last fiscal year, DENSO spent 8.8 percent of its global consolidated sales on research and development. DENSO common stock is traded on the Tokyo and Nagoya stock exchanges. For more information, go to www.denso.com, or visit our media website at www.denso.com/global/en/news/media-center/

About Infineon
Infineon Technologies AG is a world leader in semiconductor solutions that make life easier, safer and greener. Microelectronics from Infineon is the key to a better future. In the 2018 fiscal year (ending 30 September), the company reported **sales of 7.6 billion Euros with about 40,100 employees worldwide**. Infineon is listed on the Frankfurt Stock Exchange (ticker symbol: IFX) and in the USA on the over-the-counter market OTCQX International Premier (ticker symbol: IFNNY).

Editor Note « I can't take my mind off it »

The PR above was published by Infineon on 26-Nov-2018. We saw it on that day but we decided not to re-published, nothing wrong but may a little bit too much imagination on our side (after 40 years at the active front of Global Semiconductor Business that can happen)

Now after 6 months « I can't take my mind off it » because it could be a similar situation as ARM UK acquired by Softbank Japan, followed by part of Softbank/ARM sold to China and now ARM China can sell licenses to any Chinese company and out of control of ARM UK? Game over NO extra ball. May be that UK should have used their time to take good care of their Hi-Tech Industry instead off slicing UK in two piece with the BREXIT. Did Intel missed ARM?
Jan. 07, 2019: Huawei Unveils Industry's Highest-Performance ARM-based CPU see Telecom COTS World Dec. 2018

Observations about DENSO, Infineon and more in bullet style:
- Infineon: formerly Siemens Semiconductors
- DENSO (Japan) is a kind of Competitor/Partner of Bosch Automotive
- Infineon is a supplier to Bosch and DENSO
- A cooperation between Bosch and DENSO was started in 1953
- Advanced Driver Information Technology Corporation (ADIT) was set up in 2003, develops platforms for vehicle infotainment systems in Kariya, Japan and Hildesheim, Germany a large site of Bosch (I was there with a Software company to help on a large business for Linux Services). Bosch and Denso are shareholders of ADIT.
- November 2012: Bosch sells shares in Denso Corporation, 46 million shares worth approximately 1.1 billion euros sold. Proceeds will serve to finance capital expenditure in promising future areas, as well as company acquisitions
- August 20, 2014, Infineon had announced that it was to acquire International Rectifier (IR) in a deal worth approximately USD 3 billion. IR is a strong leader in power semiconductors and especially in PowerMOS and IGBT (I have been working for IR, with my teams we own a huge number of designs).
- November 2018: Infineon strengthens collaboration with DENSO but DENSO becoming a shareholder
- April 2019: Infineon most probably to acquire a large US Chip company soon!
- BEST OF THIS CENTURY could be KUKA, do you remember?

Daniel Dierickx, CEO, co-founder and Principal BD/BI Consultant at e2mos www.e2mos.com

Andes Technology Announces RISC-V Single-core and Multicore Processors with DSP Instruction Set

Hsinchu, Taiwan. – March 12, 2019 – At the RISC-V Workshop Taiwan cohosted by Andes Technology today, Andes proudly announces the debut of its 32-bit A25MP and 64-bit AX25MP RISC-V multicore processors. The A25MP and AX25MP are the first commercial RISC-V cores with comprehensive DSP instruction extension. With the addition of cache-coherent multiprocessors and the DSP ISA based on the RISC-V P-extension draft Andes donated to the RISC-V Foundation, Andes brings powerful solutions to address the new market and further enriches its RISC-V lineup.

Multiple processor cores working in parallel empower applications such as artificial intelligence and Advanced Driver-Assistance Systems (ADAS) to boost performance of their computation intensive tasks significantly. Furthermore, hardware managed cache coherence simplifies software design considerably for systems with multiple CPUs. The A25MP and AX25MP support up to four CPU cores. They provide efficient cache coherence among private level-1 caches; include an optional shared level-2 cache; and support I/O coherence for bus masters without caches. Operating at over 1GHz in 28nm process with Linux symmetric multiprocessing (SMP) support, the A25MP and AX25MP raise the RISC-V processors to the next performance level and a wider market.

Many embedded applications processing digital signals such as voice, audio and image require efficient DSP instruction set as general-purpose baseline instructions are often not sufficient. As a founding member of the RISC-V Foundation, Andes responded to the popular inquiries for DSP capabilities in the RISC-V ISA by chairing the P-extension Task Group of the RISC-V Foundation, and donating its industry proven DSP/SIMD ISA to kick start the standardization effort. Andes' new A25MP and AX25MP cores support the P-extension draft. Accompanying the DSP-capable processors are complete supporting tools including compiler, DSP libraries and simulator. Together they enable an over 7 times acceleration in the PNET for MtCNN (Multi-task Cascaded Convolutional Networks) face detection and alignment algorithm. They also provide an order of magnitude performance boost on CIFAR10 image classification benchmark for machine learning, which is a collection of images commonly used to train machine learning and computer vision algorithms.

"For over a decade Andes remains a major CPU IP vendor, and a leading supplier of RISC-V cores including the new N22-series and N25-series cores that serve the ever increasing demand for ultra-compact and high-performance RISC-V processors," Andes President Frankwell Jyh-Ming Lin said. "Over 150 companies have licensed AndesCore™ processor IP and billions of electronic devices containing Andes CPU IP in a wide variety of applications have shipped globally."

"The introduction of A25MP and AX25MP RISC-V multicore is a significant advancement for both Andes and the RISC-V community," said Dr. Charlie Su, CTO and EVP of Andes Technology, "Built upon Andes' successful processor solutions and solid development support, these powerful multiprocessor IPs with sophisticated DSP instructions as well as floating-point instructions mark the RISC-V architecture's major step forward in the processor industry. It is truly exciting that Andes RISC-V solutions are being rapidly adopted by the industry since their introduction. We encourage the world to benefit from the developments pioneered by the RISC-V Foundation including Andes Technology."

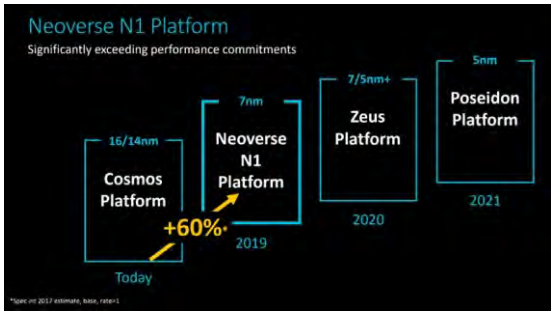
Along with the introduction of A25MP and AX25MP, their single-core versions, the previously released 32-bit A25 and 64-bit AX25 with Linux and floating-point support, are now upgraded with the DSP ISA. Also made available is the 32-bit D25F processor, which is an A25 without MMU and S-mode support to closely address DSP applications which do not need to run Linux. All these processor IP's enjoys the same efficient baseline pipeline of the 25-series processors and the powerful ACE tools for custom instruction design.

For more information about the A25MP/AX25MP multicores, the upgraded A25/AX25, the D25F, and the latest developments of RISC-V P-extension DSP/SIMD ISA, please contact Andes Technology at http://www.andestech.com/.

Arm Unveils Neoverse N1 Platform with up to 128-Cores

By Tiffany Trader HPCwire | February 20, 2019

Following on its Neoverse roadmap announcement last October, Arm today revealed its next-gen Neoverse microarchitecture with compute and throughput-optimized silicon designs catered toward general-purpose cloud computing and edge computing. The Arm Neoverse N1 platform, the first built on the 7nm "Ares" core, scales up to 128 cores and delivers a 2.5x performance improvement on key cloud workloads, according to Arm. The company's Neoverse E1 platform, also announced, debuts as a high-efficiency throughput platform, promising a 2.7x improvement in throughput performance over previous generations.



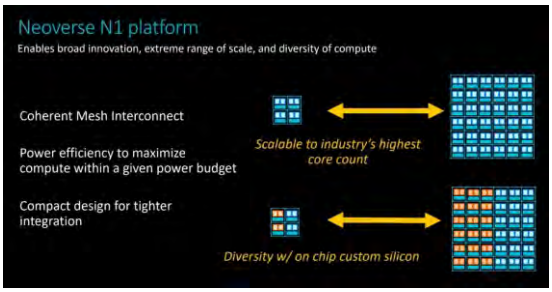
The new N1 platform (previously known by the Ares codename) is the successor to Arm's 16nm Cosmos platform, which includes the Cortex-A72, A75 and A53 CPU cores. AWS' Graviton processor, announced in November at AWS re:Invent, is based on Cosmos.

Arm reports that chips based on the N1 platform will boost integer performance by 60 percent over the Cortex-A72 Cosmos processor (measured with the industry SPEC int 2017 benchmark), overdelivering on their promise to improve performance by 30 percent year to year. N1 also yields a 30 percent power efficiency improvement over Cortex-A72, according to Arm.

"Going beyond raw compute performance, the Neoverse N1 platform was built from the ground up with infrastructure-class features including server-class virtualization, state-of-the-art RAS support, power and performance management, and system level profiling," commented Drew Henry, head of Arm's infrastructure business unit — its fastest-growing division — in a blog post. "The platform also includes a coherent mesh interconnect, industry-leading power efficiency, and a compact design approach for tighter integration, enabling scaling from 4- to 128-cores." Partners have the flexibility to add accelerators or other features with their own on-chip custom silicon, he added.

As you'd expect, Arm's Coherent Mesh Network (CMN) is key technological asset of the N1 platform. "We've been making coherent interconnects for quite some time in different markets and have evolved from cross bar to a ring and now a mesh given the core counts that we're at," Senior Director Brian Jeff told reporters last week. "Ares and the CMN were designed together to optimize the way the mesh interconnect works together with the CPU and communicates about how much data to prefetch into memory, how the cache can be used and allocated among the different cores and a lot of other features." Jeff also noted, in a blog post (offering a closer look at the microarchitecture), that the N1 system could scale beyond 128-cores, however "real systems will architect around memory bandwidth and likely come in at 64 to 96 cores with 8ch DDR4 and 96 to 128 cores with DDR5." An 8 core chip at the edge is expected to draw <20 watts while an 128 core chip for hyperscale applications is estimated at <200 watts.

In a briefing last week, Henry, senior vice president and general manager of Arm's infrastructure business, noted the company's rising momentum underscored by Top500 recognition for the world's first petascale Arm supercomputer in November. Arm is also the engine for the massive post-K supercomputer, being built in Japan this year with Fujitsu AFX64 Arm CPUs. AWS, Huawei and Ampere have all announced Arm CPUs in recent months.



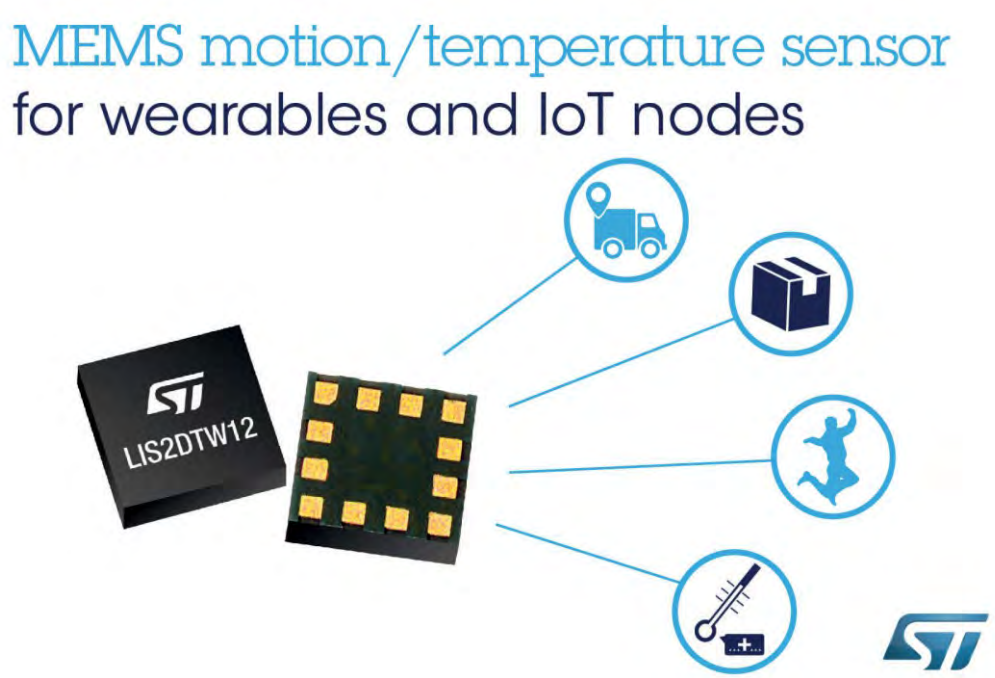
Market watchers have been looking for Arm's traction in the larger datacenter market. "Everyone has wanted to know, 'where are you guys in hyperscale, where are you in servers?'" Henry told reporters last week. With the rollout of AWS Neoverse Graviton and the launch of Arm's N1 platform, Henry wants the industry to know that the success Arm has had in other areas of infrastructure is now moving into the core datacenter. "The N1 platform is really about the core compute – the core compute you need in the hyperscale datacenter and the core compute you might need in the 5G base station or at an internet gateway," said Henry. The Neoverse E1 platform, also announced today, "was designed very specifically to put high throughput through the internet, also from the edge to the core datacenter."

"Featuring an intelligent design for highly-efficient data throughput, the Neoverse E1 achieves 2.7x more throughput performance, 2.4x more throughput efficiency, and over 2x more compute performance compared to our previous generations," said Henry. "It also delivers scalable throughput for edge to core data transport, supporting everything from a sub-35W base station all the way through to a multi-100GB router." Both the N1 and E1 designs have been available to partners for "a while," Arm said. The company expects the first silicon to come to market by the end of this year, ramping up into the following year, pending customers' schedules and timelines.

Source - Special Links - Larger Pictures CLICK HERE

MEMS Chip Combines Accelerometer with High-Accuracy Temperature Sensor for Superior Precision

The STMicroelectronics LIS2DTW12 combines a MEMS 3-axis accelerometer and a temperature sensor on a single die for use in space-constrained and battery-sensitive detectors such as shipping trackers, wearables, and IoT endpoints. The sensing accuracy of 0.8°C offers precision comparable with stand-alone standard temperature sensors.



In addition to enhanced temperature compensation, leveraging the sensor's superior accuracy, the accelerometer benefits from unprecedented flexibility with 65 different user modes that enable developers to optimize power consumption and noise to meet application-specific requirements. It has user-selectable full-scale range up to ±16g and measures acceleration with output data rates from 1.6Hz to 1600Hz.

With about 30% lower package height than other combination sensors, at just 0.7mm, the LIS2DTW12 allows extra battery capacity for longer runtimes. Power-saving features let devices go even further between charges, and include a 50nA power-down mode, multiple operating modes down to less than 1µA, a dedicated internal engine for processing accelerometer signals, and a large 32-level FIFO to reduce intervention from the main controller.

The LIS2DTW12 provides 16-bit accelerometer data and 12-bit temperature data through a high-speed I2C/SPI port, and allows single data conversion on demand. The motion engine performs free-fall and wakeup detection, single/double-tap recognition, activity/inactivity, stationary/motion detection, portrait/landscape detection, and 6D/4D orientation. ST's advanced self-test capability is also built-in to verify the sensor is functioning correctly.

The LIS2DTW12 is specified from -40°C to +85°C and available now in the ultra-thin 2.0mm x 2.0mm x 0.7mm LGA-12 plastic land grid array package, priced from $0.99 for orders of 1000 pieces.

A dedicated adapter board, STEVAL-MKI190V1, is ready to use with the STEVAL-MKI109V3 microcontroller motherboard to connect to a PC running the Unico development GUI or a custom application for inspecting the sensor data.

For more information please go to www.st.com/lis2dtw12-pr

You can also read our blog post at https://blog.st.com/lis2dtw12-accelerometer-thermometer/

Infineon New IGBT 3,3kV 450A Power Modules for Compact and Scalable Inverter Designs

Jyoti Gazmer | April 5, 2019

Infineon Technologies extends its large portfolio of high voltage devices with a new package: XHP 3. This is a new flexible IGBT module platform for high-power applications in the voltage range from 3,3 kV up to 6,5 kV.

The module allows for scalable designs with best-in-class reliability and highest power density. Due to its symmetrical design with low stray inductance, it offers significantly improved switching behavior. For this reason, the XHP 3 platform offers a solution for demanding applications such as traction and commercial, construction and agricultural vehicles as well as medium-voltage drives. The high-power platform will be showcased at **PCIM 2019**: booth #313 in hall 9 (Nuremberg, Germany, 7-9 May 2019).

Infineon's XHP 3 package comprises a compact form factor with 140 mm in length, 100 mm in width and 40 mm in height. The first IGBT modules of this new high-power platform feature a half bridge topology with a blocking voltage of 3,3 kV and a nominal current of 450 A. In order to meet customers' demands, two different isolation classes are launched simultaneously: 6 kV (FF450R33T3E3) and 10.4 kV (FF450R33T3E3_B5) isolation, respectively. Ultrasonic welded terminals and aluminum nitride substrates along with an aluminum-silicon carbide base plate ensure the highest possible level of reliability and robustness.

The high-power IGBT module is designed for paralleling and, for this reason, offers a new level of scalability. System designers can now easily adapt the desired power level by paralleling the required number of XHP 3 modules. To facilitate scaling, Infineon offers pre-grouped devices featuring a matched set of static and dynamic parameters. Using these grouped modules, de-rating is no longer required when paralleling up to eight XHP 3 devices.

For more information Click here

Infineon acquires Siltectra, a specialist for silicon carbide

Munich and Dresden, Germany – 12 November 2018 – Infineon Technologies AG (FSE: IFX / OTCQX: IFNNY) acquires Siltectra GmbH https://www.siltectra.com/, a start-up based in Dresden. The start-up has developed an innovative technology (Cold Split) to process crystal material efficiently and with minimal loss of material. Infineon will use the Cold Split technology to split silicon carbide (SiC) wafers, thus doubling the number of chips out of one wafer. A purchase price of 124 million Euros was agreed on with the venture capital investor MIG Fonds, the main shareholder.

"This acquisition will help us expand our excellent portfolio with the new material silicon carbide as well. Our system understanding and our unique know how on thin wafer technology will be ideally complemented by the Cold Split technology and the innovative capacity of Siltectra," said Dr. Reinhard Ploss, CEO of Infineon. "Thanks to the Cold Split technology, the higher number of SiC wafers will make the ramp-up of our SiC products much easier, especially regarding further expansion of renewable energies and the increasing adaptation of SiC for use in the drive train of electrical vehicles."

Dr. Jan Richter, CTO of Siltectra: "We are glad to become part of the team of the global market leader in power semiconductors. Having shown that the Cold Split technology can be used at Infineon in principle, we will now work together to transfer it to volume production."

Michael Motschmann, General Partner of MIG Fonds' administrator MIG AG, said: "Since we invested in Siltectra more than eight years ago, we have always believed in the Cold Split technology and the great team. We are very pleased that we found Infineon as a buyer who fits perfectly technologically as well as culturally to the company. Furthermore, it makes us proud that we helped to strengthen Germany's economic competitiveness by our investment." Currently MIG AG manages a portfolio of 24 companies. For further information: www.mig.ag, www.mig-fonds.de.

Siltectra was founded in 2010 and has been growing an IP portfolio with more than 50 patent families. The start-up developed a technology for splitting crystalline materials with minimal loss of material compared to common sawing technologies. This technology can also be applied with the semiconductor material SiC, for which rapidly rising demand is expected in the coming years. SiC products are already used today in very efficient and compact solar inverters. In the future, SiC will play a more and more important role in electro-mobility. The Cold Split technology will be industrialized at the existing Siltectra site in Dresden and at the Infineon site in Villach, Austria. The transfer to volume production is expected to be completed within the next five years.

Infineon offers the broadest product portfolio of power semiconductors based on silicon as well as the innovative substrates of silicon carbide and gallium nitride. It is the only company worldwide with volume production on 300 mm silicon thin wafers. Therefore, Infineon is well positioned to apply the thin wafer technology to SiC products as well. The Cold Split technology will help to secure the supply of SiC products, especially in the long run. Over time, further applications for the Cold Split technology might emerge, such as boule splitting or the use for materials other than silicon carbide.

Keep your devices cool
From small components up to large systems

Laird Thermal Systems Appoints Dr. Karine Brand as CEO

New CEO successfully led the transition to establish Laird Thermal Systems as a fully-operational, independent business owned by Advent International…

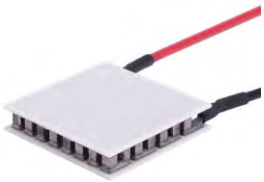
January 31, 2019 – Laird Thermal Systems, an end-to-end thermal management solution provider, has named Dr. Karine Brand as CEO, effective immediately. Dr. Brand has been a member of the management team since 2015, and recently led the transformation of the thermal system business unit into a standalone company. Dr. Brand previously served as the VP of Engineering and Technology at Laird.

Dr. Brand's efforts have established Laird Thermal Systems as the industry's leading thermal management solution provider for mission-critical and business-critical applications. Laird's diverse cooling product portfolio ranges from components and subsystems to full turnkey cooling solutions with multiple thermal technology options. With Dr. Brand's leadership, Laird Thermal Systems has built a technology and engineering team with strong technical expertise in thermoelectric modules (TEMs), thermoelectric assemblies (TEAs), liquid cooling systems (LCS) and integrated thermal management controllers. These thermal management products facilitate customer technology development by providing cutting edge solutions coupled with the ability to qualify, manufacture and service globally.

"Serving as interim CEO, Dr. Brand has been instrumental in managing the separation of Laird Thermal Systems from Laird plc and reshaping the company into a fully-operational, independent business. Dr. Brand's leadership has been paramount in this transition, and her experience and understanding of the business, technology and customers are second to none," said Roland Köppel, Chairman of the Board at Laird Thermal Systems. "I am pleased to formally announce Dr. Karine Brand as the new CEO of Laird Thermal Systems, and have complete confidence that she will lead our company to a prosperous future."

Learn more by visiting www.lairdthermal.com

About Laird Thermal Systems
Laird Thermal Systems designs, develops and manufactures thermal management solutions for demanding applications across medical, industrial and telecommunications markets. We manufacture one of the most diverse product portfolios in the industry, ranging from active thermoelectric modules (TEMs) and thermoelectric assemblies (TEAs) to temperature controllers and liquid cooling systems. With unmatched thermal management expertise, our engineers use advanced thermal modeling and management techniques to solve complex heat and temperature control problems. By offering a broad range of design, prototyping and in-house testing capabilities, we partner closely with our customers across the entire product development lifecycle to reduce risk and accelerate time-to-market. Our global design, manufacturing and support resources help customers shorten their product design cycle, maximize productivity, uptime, performance and product quality. Laird Thermal Systems is the optimum choice for standard or custom thermal solutions.



The Laird Group https://www.lairdtech.com/

- **Laird Connectivity:** • Wireless Modules • IoT Platforms • RF Antennas - IoT Solutions
- **Laird Performance Materials:** • EMC Components • Inductors • RF Absorbers • Precision Metals • Thermal Interface Materials • Wireless Charging Components
- **Laird Thermal Systems:** Thermoelectric Modules Thermoelectric Assemblies Liquid Cooling Systems Temperature Controllers Custom Solutions

GPUs and Virtualization Boost Performance for ADAS Platforms

Rapidly advancing autonomous/ADAS technologies require more powerful GPUs to handle the load. To help mitigate costs on this front, designers are turning to virtualized GPUs to perform multiple tasks.

Bryce Johnstone | Apr 05, 2019

Over the course of decades, the graphics processing unit (GPU) has evolved from its origins as a video display adapter in arcade games to a computing powerhouse that drives artificial intelligence and machine learning, accelerating computational workloads in a wide array of fields from oil and gas exploration to natural language processing. Specifically, GPUs play an increasingly critical role in the fast-evolving technologies for autonomous driving and advanced driver-assistance systems (ADAS).

How did the GPU find its way from the video arcade to the cutting edge of scientific research and self-driving cars? The GPU's rise as the go-to processor for Big Data workloads is due to some basic architectural differences between the traditional central processing unit (CPU) and the GPU. The GPU is a specialized type of microprocessor, originally designed for rendering visual effects and sophisticated 3D graphics for gaming, which requires intense computing power to display real-time action. To deliver that capacity, a GPU uses thousands of small and efficient cores to deliver a massively parallel architecture that can handle the processing of vast amounts of data simultaneously.
Over the course of decades, the graphics processing unit (GPU) has evolved from its origins as a video display adapter in arcade games to a computing powerhouse that drives artificial intelligence and machine learning, accelerating computational workloads in a wide array of fields from oil and gas exploration to natural language processing. Specifically, GPUs play an increasingly critical role in the fast-evolving technologies for autonomous driving and advanced driver-assistance systems (ADAS).

How did the GPU find its way from the video arcade to the cutting edge of scientific research and self-driving cars? In contrast, a typical CPU consists of just few cores with abundant cache memory and is usually designed to process only a few software threads at a time. CPUs are optimized for sequential serial processing, which is sufficient for most general-purpose computing workloads. However, when it comes to simultaneous processing of vast amounts of data, the GPU wins.

A GPU with hundreds of cores to process thousands of threads in parallel has the capacity to accelerate the performance of some software by 100X compared to that of a typical CPU. And increasingly, the really challenging computational problems that we expect computers to solve for us have inherently parallel structures. Think of the enormous volumes of video-processing, image-analysis, signal-processing, and machine-learning flows that must occur reliably and in real-time to operate a self-driving vehicle. In power-constrained systems like a battery-powered electric vehicle, it's also important that a GPU typically achieves this processing speed while providing more power- and cost-efficiency than a CPU.

GPUs are Tailor-Made for Autonomous Vehicles

The processing requirements of autonomous vehicles and ADAS technologies are completely within the GPU wheelhouse, especially in the areas of image analysis and parallel signal processing. Image processing is a natural problem domain for the made-for-gaming GPU. Indeed, almost any kind of computationally dense parallel computation is a good fit.

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GPUs and Virtualization Boost Performance for ADAS Platforms

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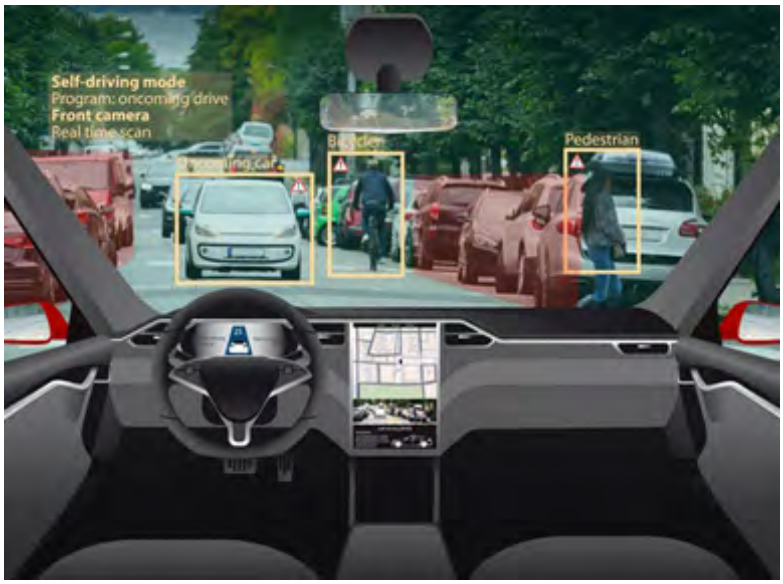

ADAS platforms can leverage the GPU's graphics compute capability to process and analyze sensor data in real-time. These discrete sensors include:
Light detection and ranging (LiDAR), which measures the distance to a target with a pulsed laser light.
Radio detection and ranging (radar), which is similar to LiDAR but uses radio waves instead of a laser.
Infrared (IR) cameras systems that use thermal imaging to perceive in darkness.

These all enable ADAS to better interpret the environment and improve the system's ability to support the driver and maintain the safety of an autonomous vehicle.

As self-driving systems become more prevalent and advanced, the GPU will increase in importance—and in power. The GPU is set to be the workhorse of the autonomous vehicle, as it will be able to deliver the compute capabilities to enable cars of the future to become more aware of and responsive to their environment so that they can operate dependably, efficiently, and safely.

Virtualizing the GPU

The level of performance demanded by ADAS platforms will require increasingly larger and more powerful GPUs, thus impacting the manufacturing bills of materials for autonomous vehicles. To mitigate this expense, platform vendors will look to increase the value and functionality of the GPU by using it to perform multiple workloads in the vehicle.

Most modern vehicles already have GPUs on-board to enable driving displays and other digital dashboards, with multiple high-resolution screens to show maps, forecasts, and other visual information. 1080p resolution is now common in mid-range cars and 4K screens are increasingly specified for luxury and executive cars.

As we've already discussed, a single physical GPU is already capable of tremendous processing performance. However, virtualizing the GPU using specialized software abstracts the processing potential of a physical GPU and transforms it into multiple virtual instances. A single physical GPU is able to host multiple virtual workloads, all operating independently of each other yet emanating from the same hardware. Virtualization lets the GPU run multiple autonomous operations, without any of the virtual instances being aware of each other or in any way affecting the others.

Virtualized GPUs have obvious applicability for autonomous vehicle and ADAS scenarios, as a single GPU can power multiple applications, from visualization of maps and operations of entertainment consoles to the processing of environmental sensor data to identify roadway obstacles.
However, enabling multiple virtual operations from a single GPU in automotive applications is only safe and effective if the GPU has rock-solid support for hardware-accelerated virtualization.

Virtualization software is most dependable when hardware enforces entirely separate managed address spaces for each virtual instance, and enables the restart, or flushing, of an instance that's not operating correctly. This workload isolation is key to allowing shared use of the GPU, while keeping critical software, such as driver-assistance systems, from being corrupted by any other process.

Imagine a situation where a problem with the dashboard software was able to affect the correct operation of the drive-assistance system—it would have disastrous consequences. Hardware-supported virtualization for GPUs provides protected execution contexts to ensure that this situation doesn't arise.

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GPUs and Virtualization Boost Performance for ADAS Platforms

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From an ADAS platform developer's point of view, hardware-based virtualization offers another additional benefit. It enables a safer environment to deliver various applications and services without any concerns about the electronics systems being taken down by a rogue piece of software. It also means that rather than a traditional hardware box with fixed software for the infotainment and engine management systems, the car becomes a flexible, configurable software platform that can be updated over-the-air. It enables OEMs to swap paid-for services in and out easily, without disrupting the car's operation, thus offering potential new revenue streams.

Imagination's GPU Solutions

PowerVR GPUs developed by Imagination Technologies address the data processing and trusted architecture challenges that face developers of autonomous-vehicle platforms. PowerVR GPUs support full hardware virtualization, completely isolating virtual instances that share the GPU. They also provide the muscle required to manage and prioritize these virtual operations to effectively power the ADAS platform architecture, with the performance bandwidth demanded to achieve safe, dependable outcomes.

Lower power consumption is also critical for autonomous vehicles, as most self-driving cars will be electric and operate on batteries. Lower power requirements for the vehicle control computing platform help lead to improved overall vehicle performance.

The core compute architecture inside PowerVR GPUs was designed from the ground up to offer fast performance and low power consumption through reduced-precision computation, especially half-precision floating point (Fp16). Running at lower precision (where lower is usually classed as less than 32 bits) is one of the best ways to reduce power dissipation in an embedded GPU without significant loss of accuracy.

Imagination designed the FP16 hardware as a separate data path from the full-precision FP32 hardware. Though shared data-path designs are common since they're simpler in many ways, having discrete hardware for each pathway enables the company to offer the best possible power consumption and efficiency as each data path accepts fewer design compromises to do what it needs to do.

Imagination also offers a toolset to support the development, optimization, and deployment of neural networks across GPU and AI accelerators. The design environment provides a single unified tool-chain that lets developers take multiple frameworks and multiple network types and bring them into a format that allows them to be deployed on:
The GPU as a compute engine.
The PowerVR Series2NX and Series3NX neural networks accelerators.
A mixture of the above two, where the flexibility of the GPU to implement a new network layer can be complemented by running the remaining layers on a highly optimized, high-performance dedicated convolutional-neural-network (CNN) accelerator.

According to Imagination, ADAS platform designers can trust PowerVR GPU as a proven component in the overall system architecture of the autonomous vehicle, with best-in-class power efficiency and memory bandwidth usage, as well as a balanced GPU design that fits well with the car's technology needs. These include improved performance for the systems that the driver and passengers interact with most—on larger and higher-resolution displays—and with a design that lends itself to safer, more dependable next-generation ADAS applications.

By: Bryce Johnstone is Director of Automotive Segment Marketing at Imagination Technologies.
Source: Imagination: https://www.imgtec.com/
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Digital Twins Deciphered

It's easy to see a digital twin as nothing more than a simulation model, but that would ignore a very important difference.

March 28th, 2019 - By: Brian Bailey
SEMICONDUCTORENGINEERING https://semiengineering.com/digital-twins-deciphered/

Ever since Siemens acquired Mentor Graphics in 2016, a new phrase has become more common in the semiconductor industry – the digital twin. Exactly what that is, and what impact it will have on the semiconductor industry, is less clear.

In fact, many in the industry are scratching their heads over the term. The initial reaction is that the industry has been creating what are now termed digital twins for the past 30 years. In some ways, they're correct.

Suitable definitions can be found from a paper from the aeronautics, aerospace and defense industry:
◦A digital twin is a digital representation of the current state of a manufactured product or system at any given point in time.
◦A digital thread is a digital record of all states of a manufactured product or system over time from conception to disposal.

Within the context of the semiconductor industry, Frank Schirrmeister, senior group director for product management and marketing at Cadence, defines the term as it applies to an emulation product. "A digital twin is a digital representation of a product or system under development representing a functionally correct, predictable and reproducible representation of the product or system at the appropriate level of fidelity to perform verification, performance analysis and system validation tasks."

Many add another important distinction. "Conceptually, it also integrates data from the actual operation of the system in the field," says Roland Jancke, head of design methodology for Fraunhofer IIS/EAS. "Thereby the models are improved, and operation strategies are adapted. The digital twin learns throughout the whole lifecycle and hands that knowledge over to its real-world twin."

In addition, some things are better in the virtual world. "Using a combination of data and simulation you can improve monitoring by adding virtual sensors," adds Sameer Kher, director for systems and digital twins at ANSYS. "For example, this enables you to add temperature probes into an IC where there is no physical way to measure it."

Much of this may sound very familiar to people in the semiconductor space. "You take the behavior of a chip, be it function, thermal, mechanical, CFD—all of the various processes of the chip—that is the entire purpose of the EDA industry," says Joe Sawicki, executive vice president, Mentor IC EDA at Mentor, a Siemens Business. "Providing digital twins for behavior is done so that it can be simulated, validated, and you can predict the yield of the device."

Others agree. "Are you trying to design the electronic system, or are you trying to develop software for that system, are you trying to validate that software with real-world connections in a real environment, perhaps using an FPGA prototype?" asks Marc Serughetti, senior director of business development and product marketing for automotive solutions in Synopsys. "The key is that a digital twin is the means to an end."

Digital twin scope
The concept of a digital twin has been used in chip design almost since the first integrated circuits. "Plan and develop a model instead of the actual circuit, and make sure both show the same behavior when stimulated with the same signals," says Fraunhofer's Jancke. "You may even develop the software using the model and trust that it will run on the hardware as well. These principles are inevitable in the design of today's multi-billion-transistor designs."

The reason why we are now hearing the term digital twin is because of the increasing scope of the EDA and semiconductor industries. "At the highest level, consider the airplane as the scope," says Schirrmeister. "The digital twin is a digital version of the design, the system, to which I can apply real-life data and do some meaningful analysis."

Automotive has been using digital twins for many years. "They have been doing it in the mechanical space and now they are looking at how they do it in the electronics space," explains Serughetti. "Ultimately, the electronic system is not independent from the mechanical system because you are trying to control something. You have to bring the mechanical twin together with the electronic twin together with the software twin—all together as you build the system."

The automotive industry should take the semiconductor industry as a guide. "They need to build a similar approach to what the semiconductor industry has done," adds Serughetti. "They want to establish a virtual development process and representation. In this case at the SystemC-level."

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Getting the right abstraction can be tricky. "It all depends upon fidelity," says Schirrmeister. "If the system is fully modeled with all of the detail, which you can never have, you get exactly the same results as the physical system. If not, you can still do some meaningful analysis at the system level looking at what the real data would mean to the digital twin."

"We often talk about hybrid emulation, which brings together RTL running on the emulation box working in parallel with a virtual prototype and that has a very different level of abstraction," says Serughetti. "What you put in the virtual prototype is not necessarily what you are trying to verify. If you take the RTL model and use it for vehicle simulation, it will not work because it is too slow. You need a different model for that."

This trend is reviving a term that fell out of favor a few years ago. "For the chip, it means electronic system level (ESL) models are needed that are abstract enough and capable of being integrated into a larger system context simulation," says Jancke. "Then the overall concept can be validated, control algorithms and operation strategies can be developed and even failure scenario run prior to real silicon."

Digital twins can be very abstract. "I can build a digital twin of the full product, which is something like the iPhone SDK," says Schirrmeister. "That is a digital twin. I can do software development on it and I can apply the data from a real design to see if I get a phone call while playing Angry Birds and getting a calendar invite—will it actually do something wrong."

Obtaining value

Rarely does significant value come from improving a capability that already exists. Only when a completely new capability is offered does it becomes really interesting to the industry.

"If you are doing a networking chip, you can run packets through it all day long," says Sawicki. "It is easy to do within your digital verification environment. Same thing for a CPU. I can boot an operating system, run applications and that is sufficient. But when you are talking about something running against a LiDAR array, some imaging, some other sensors running alongside a braking system—that is where people became very interested in grabbing our digital twin for the processing element so that they can do more significant verification. Does this start to find issues that you could not find without it? There is an awful lot of engineering being bet on that."

A digital twin manages all that data. "The amount of data that you have to look at becomes so big that you cannot make sense of it with a physical system," says Serughetti. "This is why you need the digital twin. In a digital environment you have more facilities to aggregate data to do simulation, etc."

Schirrmeister agrees. "We are increasing the scope to a level where no human being can understand it in their heads. It comes down to the specific tasks that they will get used for. What I am building is a specific subset and a very specific fidelity with specific interfaces into the real world and doing it in a way that is much easier than in the real world."

The business value needs to be obvious. "We use it for failure prediction," says ANSYS' Kher. "Using simulation, we can predict steady state temperature or behavior and what that would mean in terms of failures. It also enables 'what if' analysis that can be used to perform optimization. Given the current set of operating conditions, using the offline digital twin we can predict and optimize behavior of the physical equipment."

Not just simulation

A simulation model is one form of digital twin, but data can also be a digital twin. "Simulation is when you want to see the behavior," says Serughetti. "Imagine that I am someone who is trying to aggregate data associated with wiring in the car. My digital twin does not require mechanical or behavioral information, it may only require knowing how things are connected with each other. So there is the concept of a digital twin to meet a certain objective."

It also may be limited to a specific part of the design flow. "You may be satisfied drawing correlation based on data where you do not need a digital insight from simulation," says Kher. "It may be because it is straightforward. Pure data may get you 60% level of accuracy in terms of predictions, and may be appropriate for some cases. But when you do need more insight and you need physics, that is when simulation-based digital twins come in."

Bills of material (BoM) represent another type of digital twin. "The F35 is integrating 200,000 parts from 1,600 suppliers using 3,500 integrated circuits and 200 unique chips with more than 20 million lines of software," says Schirrmeister. "There are tools for automotive where you can look at the part numbers. From the VIN number, I want to identify if cars with this particular chip in it, for which there are three suppliers, fail more often than others? That is an analysis I can do in my digital twin by applying the real data."

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Extending into production

Some of the concepts are being utilized closer to home. "You also can think about a digital twin in the manufacturing process," says Serughetti. "The twin plays a role where the problem is how to optimize the manufacturing process."

This was a focus of the DVCon keynote speech given by Fram Akiki, vice president of electronics industry strategy at Siemens PLM Software. "When we consider the concept of first time right for a design, imagine the importance of having an equivalent first time right for a semiconductor production facility. When looking at a 7nm, 300mm facility that costs upwards of $15B, before you actually want to physically implement that you'd better have a really good virtual, digital model of how this facility will be built and optimized."

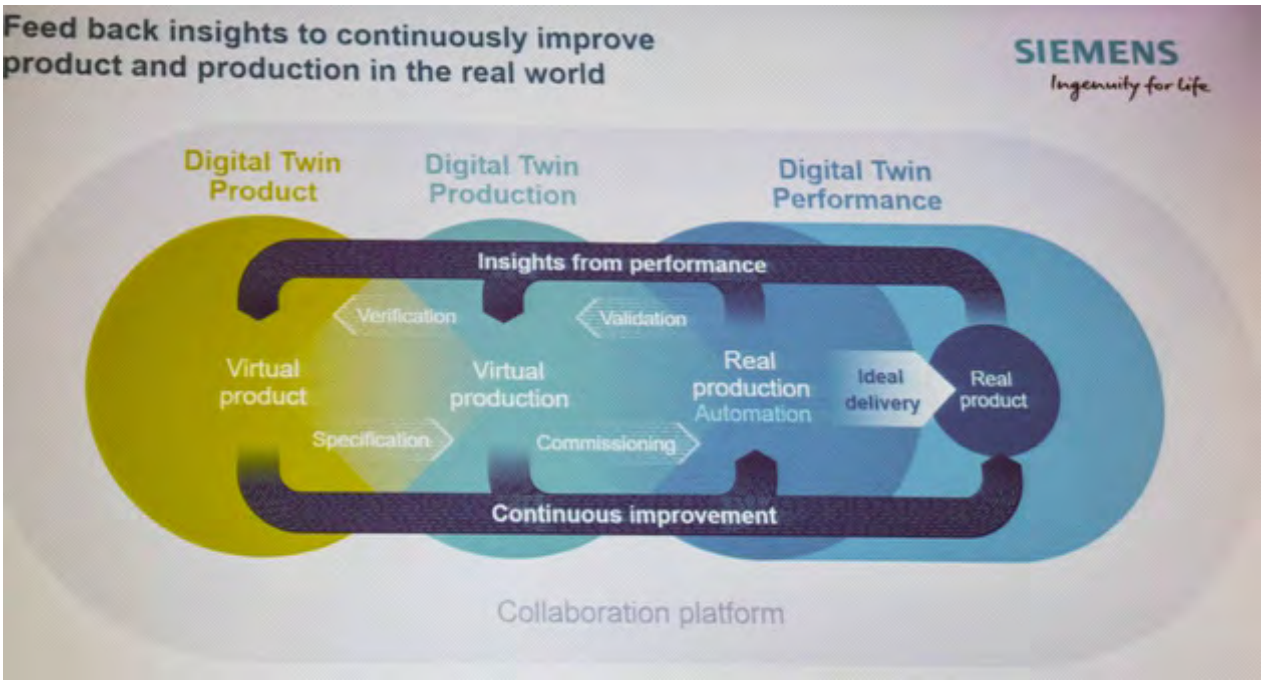

Fig 1: Extending the concept of the digital twin into production. Source: Siemens

Akiki pointed out the boundaries between the stages are blurring and dissolving. He believes that design has to become more sensitive to production capabilities and the potential costs associated with using particular capabilities.

In many cases, equipment within a production sense also can benefit from a digital twin. "We have built a digital twin for plasma-enhanced chemical vapor deposition (PECVD)," says Kher. "We need a detailed computational fluid dynamic (CFD)-based thermal analysis of the equipment augmented with some of the controls. When new vapor is injected, the temperature can change at the surface of the wafer, so it is important to regulate and monitor that. This is an application where a digital twin that essentially focuses on the surface temperature of the wafer has to model some of the external inputs around it."

Building the digital twin

Most models built for chip design are directly in the development path of the product. As an industry we understand the problems associated with integrating disparate models together, especially when they employ different abstraction or physics. "There is no one homogeneous platform or environment," points out Kher. "There is a heterogeneity of solutions and system. Simulation-based digital twins have to integrate into whatever operational platform exists. For a factory, that may be a manufacturing execution system (MES), etc. This can be tricky to figure out which one to integrate into. There is some integration work required."

It is made more difficult when models have to come from multiple sources. "Several models from different suppliers in multiple languages using diverse simulation principles have to be integrated into a single efficient simulation model," adds Jancke. "This poses tough requirements on the interfaces between the individual parts and the overall framework."

Some companies help with the creation of digital twins. "We do create virtual prototypes for several semiconductor companies," says Serughetti. "Then we go to their customers and they have a different definition for the system, which is the SoC, a microcontroller and board components. They want tools that enable them to create it independently. But it does take a lot of expertise to bring those models and simulation together."

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Model availability is a problem. "The problem with virtual prototypes is timing," says Sawicki. "This is not about clock cycles; it is about when you can actually get the model. By the time you have put together a model that has sufficient accuracy to have value in that overall system run, it is so far down the process that it no longer helps you. RTL may not be the natural behavioral level to be simulating, but it is available when you need to be simulating it. Emulation allows you to be able to get a meaningful number of simulations through the system."

Model maintenance is another issue. "Until we have a flow where there is a golden entry model—where everything flows automatically out of it—I will have some nasty effects with the early representations," says Schirrmeister. "I will never update the virtual platform to keep in sync with the actual implementation. I need to automatically create the actual twin so that everything in the digital twin manifests itself in the actual twin. The digital twin may not have the right fidelity, it may not be in sync functionality-wise. If I updated some registers, my digital twin might break because the software may not run on it. So I need to go to higher-level modeling. The challenging problems still exist."

This may not be a problem for some of industries most interested in the digital twin. "They may use model-based system engineering (MBSE), which is used to map the requirement through the engineering process into the actual simulation artefacts and then all the way back into the system," says Kher. "How do we make sure that any changes are being propagated back to the requirement so that the generated models are valid? I don't think you have to solve the entire problem in order to get digital twins. You need to build these system-level models as part of the engineering and validation phase, where you are combining the chip with software, with thermal models—whatever the pieces of information you have at the system level—in order to meet the original requirements."

Kher does have some good news on the model front. "Gradually, as models start to flow through the chain, you will see more adoption, and eventually [models] may become requirements. Bigger companies may require their suppliers to generate twinable models. It is coming, but initial success tends to be equipment manufacturers that can extract their business model to add services to their customers."

Conclusion

The EDA industry can approach this in one of two ways. It can assume we have all of the answers and try to push existing solutions into the rest of the industry, or it can listen to them and learn about their specific needs, perhaps creating some better model development flows.

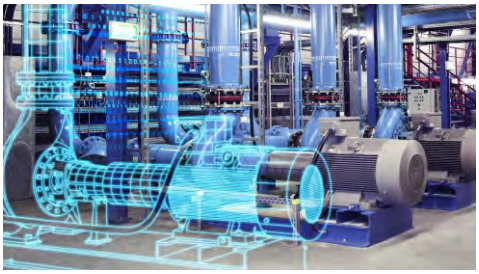
"We are taking many of the same techniques that have been used on the IC side and applying them upstream into a system context," said Akiki. "It is not just about linking digital twins and digital threads into a digital fabric, although being able to take that expertise and deploy it upstream into a system is proving to be powerful. There are some reverse techniques that also are happening, where we have looked at certain issues from a system perspective in a behavioral model, that have application in SoC development—particularly as it relates to things such as functional safety."

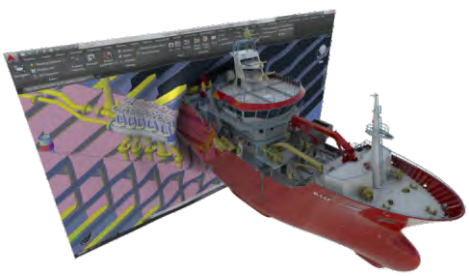
We all need to learn. "Some principles still need to be introduced into the world of IC design, such as improved simulation models from field data," points out Jancke. "We also see value in Portable Stimuli from concept level through circuit design to test equipment, to name only a few."

The key to understanding digital twins is the application of real data. "Each problem may have a specific set of techniques and capabilities that have been built over the years that we can draw on," says Kher. "We need to be able to capture real data and use it to validate quickly."

Brian Bailey (all posts)
Brian Bailey is Technology Editor/EDA for Semiconductor Engineering.

Pictures of DigitalTwin





BYD China Automotive Selects Analog Devices' Audio Bus and Processor Technologies to Improve Vehicle Energy Efficiency and Enhance Infotainment Experience

AHEAD OF WHAT'S POSSIBLE™

Feb 4 2019 - Norwood, MA
BYD and ADI PartnershipAnalog Devices, Inc. (Nasdaq: ADI) today announced that BYD Co., Ltd, a Chinese automotive manufacturer, has selected ADI's Automotive Audio Bus (A2B®) and SHARC® digital signal processor (DSP) to build more energy efficient and eco-friendly vehicle platforms while enhancing the immersive audio entertainment experience for drivers.

ADI's audio bus and DSP technologies will further enhance the performance of BYD's automotive cabin infotainment systems, providing a better driver experience, reducing the complexity and cost of design, and improving fuel/battery efficiency, which is consistent with BYD's philosophy of "technological innovations for a better life."

"BYD is a highly respected and innovative automotive manufacturer," said Mark Gill, vice president, Automotive at Analog Devices. "BYD's use of ADI's A2B and SHARC processor technologies will enable this automotive leader to offer greater energy efficiency and superior audio sound quality to its customers."

Reducing the weight, cost, and design complexity of vehicles is a major challenge faced by automotive manufacturers today. BYD has adopted ADI's A2B technology due to its ability to distribute audio and control data together with clock and power over a single, unshielded twisted-pair wire – reducing cabling weight by up to 75 percent, which improves automotive fuel efficiency and reduces total system costs. BYD also selected Analog Devices' SHARC processor to achieve more cost-effective audio systems with enhanced sound quality.

To learn more about ADI's A2B technology, visit: http://www.analog.com/a2b
To learn more about ADI's SHARC processor, visit:
https://www.analog.com/en/products/audio-video/audio-signal-processors/sharc.html

About BYD
BYD is a high-tech company devoted to technological innovations for a better life. BYD has played a significant role in industries related to electronics, automobiles, new energy and rail transit. From energy generation and storage to its applications, BYD is dedicated to providing zero-emission energy solutions.

NXP and Identiv Make IoT Applications More Accessible with Ultra-Low-Cost NFC Inlay

New Cost-Effective, High-Performance Inlay Designed for Customer Engagement NFC Applications

Austin, Texas – February 28, 2019 – Today, NXP has announced an ultra-low-cost radio frequency identification (RFID) inlay in collaboration with Identiv. Using NXP's near field communication (NFC) IC NTAG® 210µ, Identiv's Dry Inlay (25 mm diameter) has launched at a price of $0.05 a tag for a minimum order of 20Ku. Compatible with any Android or Apple iOS 11 and up NFC-enabled device, the inlay is ideal for enabling NFC use cases including Internet of Things (IoT) and customer engagement applications.

The Identiv Dry Inlay design (chip + antenna + epoxy glue + [PET] film) or wet (adhesive backing) inlays can be directly embedded in or converted into finished products. Ideal applications for the new inlay include the Internet of Things (IoT), NFC smart posters and billboards, libraries, event and transportation ticketing, automotive and chemical industries, logistics and supply chain, asset management, pharmaceuticals and healthcare, fast-moving consumer goods, beauty care, spirits, device authentication and counterfeit protection, electronic games, event management, wearable technology, and customer loyalty programs.

Quality, off-the-shelf connectivity at ultra-low costs

With over two billion NFC reader-enabled devices deployed globally, NXP's NFC Forum compliant NTAG® 210µ is designed to facilitate the adoption of NFC technology across markets in which contactless technology has typically been cost-prohibitive.

Availability and pricing

Identiv's NFC tags are available for purchase now in the Identiv webshop. Identiv's full RFID, NFC, and inlay portfolio can be viewed here and questions can be directed to nfc@identiv.com.

For more information about NXP's NFC IC solutions, please visit: www.nxp.com/nfc

New Arm technology will strengthen driver trust on the road to safe mass autonomous deployment

By Lakshmi Mandyam, VP automotive, Arm | December 18, 2018

News highlights:
- Arm introduces latest addition to the Arm Safety Ready program, a new "Automotive Enhanced" processor designed to help enable safe next generation driver experiences
- Optimized for 7nm: Cortex-A65AE is Arm's first multithreaded processor with integrated safety for handling sensor data in autonomous and high throughput needs in IVI/cockpit systems
- **Simultaneous multithreading** optimized for high throughput workloads and offers best performance efficiency

According to recent data from AAA, 73% of American drivers are too afraid to ride in fully self-driving vehicles and 63% of US adults feel less safe sharing the road with self-driving vehicles while walking or cycling. Human acceptance of new advanced driver assistance systems (ADAS) and increasingly autonomous technologies will only happen if drivers and passengers feel safe relying on them.

Winning the trust of consumers is critical, and to deliver these trusted experiences carmakers need solutions that achieve the right balance of innovation and safety while being deployable, scalable and ready for mass production. In my regular conversations with leading OEMs and tier ones, it's clear that a broad range of compute is required to meet the needs of tomorrow's vehicles, and one size will not fit all when it comes to the compute powering these vehicles.

Earlier this year Arm demonstrated its commitment to accelerating the deployment of safe fully autonomous vehicles for OEMs and tier ones with the launch of our Safety Ready program and a dedicated range of Automotive Enhanced IP, including the Cortex-A76AE, which delivers the processing performance required for autonomous applications while changing the game with integrated safety. Today, to further expand our Automotive Enhanced IP portfolio, we are announcing the release of Arm Cortex-A65AE, formerly known as Helios-AE on our product roadmap.

Cortex-A65AE: First multithreaded processor with integrated safety
The Arm Cortex-A65AE (Automotive Enhanced) is the latest addition to Arm's Automotive Enhanced portfolio of IP, designed for more efficient processing of the multiple streams of sensor data being generated in next generation vehicles, and to help enable innovative new driver experiences safely. It does this by delivering enhanced multithreading capability combined with integrated safety through our innovative Split-Lock technology.

In order to achieve higher levels of autonomy, there will be a large increase in the number of sensors monitoring the surroundings of the vehicle, including cameras, LiDAR and radar, resulting in a significant increase in throughput and compute requirements to safely process this data. Multiple sensor inputs allow cars to view their environment, perceive what is happening, plan possible paths ahead, and deliver commands to actuators on the determined path.

With so much data being collected at different points of the vehicle, high data throughput capability is a key part of the heterogeneous processing mix required to enable ADAS and autonomous applications. It's also critical that safety is at the heart of these systems. The Cortex-A65AE is ideal for managing the high throughput requirement for gathering sensor data and can be used in lock-step mode connected to accelerators, such as ML or computer vision, to help process the data efficiently. But what's most critical, is that it does this with a high level of safety capability.

Alongside the increase in sensor inputs, more autonomy and advancing driver aids will dramatically change the human automotive experience. As part of this transition, there will be many more screens in our cars delivering enhanced experiences. Drivers will be informed through augmented reality head-up-displays, alerts and improved maps. Passengers will be immersed by rich video entertainment delivered by many screens throughout the car, but trust, reliability and safety are all critical to the acceptance of these new cabin experiences. Sensors will not only be sensing out, but will be sensing in, monitoring drivers. They will be able to monitor eyelid movement to detect tiredness, body temperature, vital signs and behavioural patterns to personalise the in-car experience. These capabilities require high throughput, ML processing and a lot of heterogeneous compute.

To deliver rich, immersive in-vehicle experiences efficiently, a heterogeneous compute cluster is necessary. Cortex-A65AE is Arm's first throughput focused application class core with Split-Lock. Together with Cortex-A76AE (also with Split-Lock), these cores enable the highest safety integrity level with leading performance and power efficiency.

The addition of the multithreaded Cortex-A65AE processor to the Arm automotive platform further cements Arm's bumper-to-bumper automotive leadership, and the Arm software ecosystem is ready for Cortex-A65AE, with support from Arm Safety Ready developer tools and Linux patches already up-streamed.

Accelerating a safer path to fully-autonomous driving
Per year, 5.3 trillion miles are driven in cars and light vehicles depending on Arm processors. Looking ahead, the Arm automotive roadmap includes Hercules-AE optimized for 7nm in 2019 as well as future Cortex-R solutions. Arm is transforming what's possible by extending our portfolio to deliver the broadest range of functional safety capable IP products in the industry. The entire platform is supported by the Arm Safety Ready program, drawing on our extensive experience in safety for the faster delivery of safer automotive solutions by OEMs, automotive tier ones and silicon partners.
For more information on our commitment to vehicle safety, please visit our Safety Ready page.

Fast-Dimming, 60-V Linear LED Controller Targets Automotive Lighting

High-output drive current allows the AL5816Q to drive a single LED, an LED chain, or multiple LED channels for applications such as rear-light clusters and instrument panels.

Murray Slovick Electronic Design | Apr 08, 2019

One of the latest developments from Diodes Incorporated is an automotive-compliant linear controller for LED lighting. Dubbed the AL5816Q, the device features an internal output drive up to 15 mA, which enables it to drive external bipolar transistors or MOSFETs. With an operating voltage range of 4.5 to 60 V and a low 200-mV current-sense feedback voltage, the AL5816Q can control the regulation of LED current with minimized power dissipation when compared with traditional linear LED drivers. This suits it for medium- to high-current LEDs.

The combination of a high-input voltage and high-output drive current, coupled with a high-voltage pulse-width-modulation (PWM) dimming feature, means automotive manufacturers can significantly lower BOM for a wide range of automotive applications using the part. These include rear-light clusters, interior illumination, instrument panels, and license-plate lighting.

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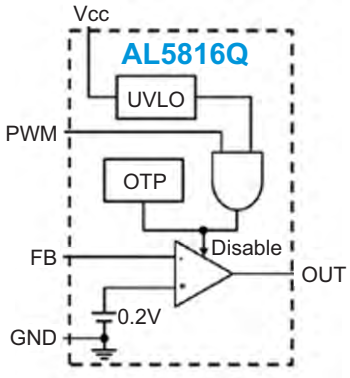
The combination of a high-input voltage and high-output drive current, coupled with a high-voltage pulse-width-modulation (PWM) dimming feature, means automotive manufacturers can significantly lower BOM for a wide range of automotive applications using the part. These include rear-light clusters, interior illumination, instrument panels, and license-plate lighting.

The high-output drive current enables the AL5816Q to drive a single LED, an LED chain, or multiple LED channels, as required, and the PWM dimming input accepts a signal operating at up to 50 kHz. Protection features include input undervoltage lockout and over-temperature shutdown.



A feedback pin operates at 200 mV, allowing the AL5816Q to control the LED drive current precisely while minimizing the dropout voltage and reducing the LED system power dissipation. The AL5816Q has LED current adjusted and controlled by a sense resistor connected across the FB pin and GND. The AL5816Q can be dimmed by a PWM signal through the PWM pin, and is able to run at frequencies higher than 200 Hz.

The AL5816Q is automotive-compliant, qualified to AEC-Q100 Grade 1 and supports Production Part Approval Process (PPAP) documentation. PPAP is used in the automotive supply chain to establish confidence in component suppliers and their production processes, by demonstrating that all customer-engineering design-record and specification requirements are properly understood by the component supplier. The PPAP is more than a paperwork task—it's a valuable tool usable by the supplier to help identify possible trouble spots in the production that's to follow.

The PPAP process is currently governed by the Automotive Industry Action Group (AIAG). It requires the manufacture of a sample number of parts on actual production tooling, using the same procedures, personnel, production facility, and all other aspects of the expected production run. This sampling is usually about 300 pieces. These are then analyzed to ensure the production run meets all of the requirements requested by the customer.

The AL5816Q is available in a SOT25 package. It's fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.

Wind River Ranked Global Leading Provider of Embedded Operating Systems

NEWS HIGHLIGHTS

- Wind River ranked as the continued global market share leader in categories of real-time operating system, commercial embedded Linux, embedded hypervisors, and safe and secure operating systems according to latest reports from VDC Research.
- Reports recognize VxWorks and Wind River Linux, along with company's virtualization and multi-tenant VxWorks safety products.
- Wind River uniquely positioned with its comprehensive software portfolio that supports a diverse range of customer journeys, from design to development to deployment.

ALAMEDA, CA – March 12, 2019 – Wind River®, a leader in delivering software to critical infrastructure, announced its achievement as the continued embedded real-time operating system (RTOS) and commercial Linux revenue leader according to VDC Research. The company also ranked as the leading commercial provider of both embedded hypervisors and safe and secure operating systems.

In VDC's latest report, "The Global Market for IoT & Embedded Operating Systems," Wind River retains its longstanding position as the market share leader for VxWorks® and Wind River Linux. The report covers the global market for commercially available RTOSs, non-real-time operating systems, and other related bundled products and services. In an additional VDC report, "2019 Hypervisors, Safe & Secure Operating Systems," Wind River also ranked as the leading provider of both embedded hypervisors and safe and secure operating systems for its virtualization and multi-tenant VxWorks safety products.

"The market for IoT and embedded OSes is changing as new open source and free initiatives enter the market," said Roy Murdock, analyst at VDC Research. "Wind River continues to lead the RTOS, commercial Linux, and safe and secure markets by adapting its comprehensive commercial offerings to suit growing safety-critical and virtualized workload demands."

"Wind River's nearly four-decade heritage as a technology pioneer and the safety, security, and reliability our software delivers to our customers continue to further solidify our position as the market leader," said Michel Genard, vice president of product at Wind River. "As industries from aerospace to industrial to automotive evolve and modernize, Wind River's edge portfolio is poised to address today's dynamic and diverse market challenges to ensure our customers' success in the emerging software-defined world."

With its comprehensive software portfolio, Wind River supports a diverse range of customer journeys from design to development to deployment, whether teams require open source and require Linux, or an RTOS, or both. This flexibility allows companies to deliver innovative products that leverage the latest community driven innovations while meeting the safety, security and reliability requirements for mission-critical applications.

This market recognition comes on the heels of Wind River expanding its product portfolio with the introduction of Wind River Helix™ Virtualization Platform, which combines VxWorks along with its hypervisor technology, Wind River Linux, and Wind River Simics® into a software edge compute platform for designing and implementing a range of mixed-criticality application options at the edge.

About Wind River

Wind River is a global leader in delivering software for the edge. The company's technology has been powering the safest, most secure devices in the world since 1981, and is found in more than 2 billion products. Wind River offers a comprehensive portfolio, supported by world-class global professional services and support and a broad partner ecosystem. Wind River software and expertise are accelerating digital transformation of critical infrastructure systems that demand the highest levels of safety, security, performance, and reliability.

To learn more, visit Wind River at www.windriver.com.